

semiconductor element, said portion extending completely around the primary surface of said semiconductor element.

as best

5. The semiconductor device according to claim 1, wherein said adhesive layer is smaller in size than the primary surface of said circuit board.

6. The semiconductor device according to claim 1, wherein said adhesive layer extends outside an outer edge of the primary surface of said semiconductor element without reaching an outer edge of the primary surface of said circuit board.--

REMARKS

Claims 1-3 stand rejected under 35 U.S.C. § 103 over admitted prior art ("APA"; Figures 4 and 5 of Applicants' drawings) in view of Amagai ('102) and Jiang et al. ('755). Claim 1 is the sole independent claim. This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "an adhesive layer which is greater in size than the primary surface of said semiconductor element" The Examiner admits that "APA . . . fails to specify using an adhesive layer which is of greater size than that of the primary surface of the element" (see outstanding Office Action, page 3, lines 3-6). The Examiner therefore relies on Amagai for allegedly disclosing "an adhesive layer (8 in Fig. 7) which is of greater size than that of the primary surface of the element (1 in Fig. 7) to improve rigidity and to reduce stress in a chip size package (Col. 6, line 25-45)." Consequently,

the Examiner substitutes the adhesive layer 5 of APA with the alleged adhesive layer 8 of Amagai.

However, it is respectfully submitted that the proposed combination is improper because it fails to provide a proper motivation and rationale *from the prior art* for making the combination. Instead, it is respectfully submitted that the Examiner has made the combinations based solely on improper hindsight reasoning, whereby the Examiner selected bits and pieces from the different prior art references and used only Applicants' specification as a guide to reconstruct the claimed invention. Specifically, the Examiner's alleged motivation for making the combination (i.e., improving rigidity and reducing stress) is improperly derived solely from Applicants' specification (*see, e.g.*, page 6, lines 5-11 and/or page 8, lines 24-28 of Applicants' specification).

The portion of Amagai relied on by the Examiner (i.e., col. 6, lines 25-45) is completely silent as to the purpose of forming the *adhesive 8* wider than the semiconductor element 1. In contrast, Amagai is directed to forming the *insulating substrate 3* wider than the semiconductor element 1 so as to increase the number of solder bumps 11. The adhesive 8 just happens to match the size of the substrate 3 in the semiconductor device disclosed by Amagai without any express discussion of benefits for having the adhesive match the size of the substrate. Accordingly, Amagai provides no motivation or rationale for using specifically a wider adhesive, and at best, merely suggests using a wider insulating substrate. However, the semiconductor device of APA *already has a substrate 1 that is wider than the semiconductor element 10* (as arguably suggested by Amagai), thereby eliminating any possible combination based on the teachings of Amagai. Contrary to Amagai, APA uses an adhesive that matches the size

of the semiconductor element 10 as opposed to the substrate 1, and the Examiner has not provided any rationale from the prior art for modifying APA by using an adhesive that matches the size of the substrate.

In summary, it is submitted that if anything, Amagai only motivates one of ordinary skill in the art to make an "insulating substrate wider than [a] semiconductor chip 1 [so as to] increase the number of solder bumps 11 that can be assembled without changing the pitch" (see col. 6, lines 36-39). Amagai provides no motivation or suggestion for specifically using a wider *adhesive*. As evidenced by APA, a wider substrate 1 can be formed without forming a corresponding wider adhesive. Accordingly, the present record provides no objective evidence that the cited prior art suggests the desirability of the proposed combination. Furthermore, as APA already has a wider substrate 1 than the semiconductor element 10, the only motivation derived from Amagai (i.e., forming a wider substrate) becomes cumulative to APA.

As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the proposed combination using *objective* evidence. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that APA can be modified by Amagai, it is submitted that the "mere fact that [APA and Amagai] can be combined ... does not render the resultant combination obvious" because nowhere does the *prior art*

"suggest the desirability of the combination" as set forth by the Examiner. The examiner has not provided any *objective* evidence that the *cited prior art* suggests the "desirability of the combination" as required for a proper rejection under 35 U.S.C. § 103. Rather, at best, the Examiner attempted to show only that the individual elements of the combination recited in claim 1 are known in a plurality of different references. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levingood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that APA and Amagai "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no *objective* reason on the record to combine the teachings of the cited prior art in the manner set forth by the Examiner. In contrast, APA and Amagai are completely silent as to providing a rationale or motivation for combining the teachings thereof. The only motivation set forth by the Examiner to make the proposed combination was derived solely from various portions of Applicants' specification (examples provided above).

Based on all the foregoing, it is respectfully submitted that claim 1 and its dependent claims 2-3 are patentable over APA in view of Amagai and Jiang et al. (Jiang et al. relied on for claim 3). Accordingly, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. § 103 over APA in view of Amagai and Jiang et al., be withdrawn.

NEW CLAIMS

New dependent claims 4-6 are submitted to be allowable based on their own merits, in addition to being dependent on novel claim 1. For example, claim 4 defines an "adhesive layer [that] includes a portion which extends radially outward relative to the primary surface of said semiconductor element, said portion extending *completely around* the primary surface of said semiconductor element" (emphasis added; *see, e.g.*, page 6, lines 26-30 of Applicants' specification). In contrast, Amagai, which the Examiner relies on for the alleged "adhesive layer", expressly discloses that "the width in the longitudinal direction of insulating substrate 3, that is, the depth shown in the figure, is ... *equal to the width of semiconductor chip 1*" (emphasis added; *see* col. 6, lines 40-44). It is therefore submitted that Amagai does not disclose or suggest the limitation recited in claim 4. Similarly, none of the cited prior art discloses or suggests the *combination* of an "adhesive layer which is greater in size than the primary surface of said semiconductor element [and] smaller in size than the primary surface of said circuit board" as recited in claim 5, nor an "adhesive layer [which] extends outside an outer edge of the primary surface of said semiconductor element without reaching an outer edge of the primary surface of said circuit board" as recited in claim 6.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, APA, Amagai, and/or Jiang et al. fail to "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 4-6 because any combination therebetween would fail the "all the claim limitations" standard required under 35 U.S.C. § 103.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
MCDERMOTT, WILL & EMERY

for *Stephan A. Becker* #46,692
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:MWE
Date: February 4, 2002
Facsimile: (202) 756-8087

Fig. 3

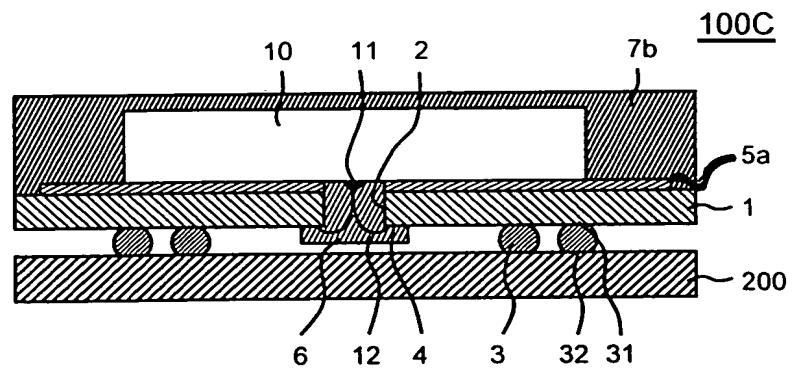


Fig. 4

Background Art

